| Notice of Allowability | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/780,023 | SAKURAI ET AL. | |
| | Examiner | Art Unit | |
| | Khanh Dang | 2111 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--*

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *6/21/2007*.

2. ☒ The allowed claim(s) is/are *1-19*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
**THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.**

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS ( as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review ( PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   **Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).**

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

**Attachment(s)**

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☒ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☐ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

Khanh Dang

**Khanh Dang**
**Primary Examiner**

## EXAMINER'S AMENDMENT

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Mr. Stephenson on July 19, 2007.

The application has been amended as follows:

**Claim 6 (Amended).**

An apparatus comprising:

a PCI data bus;

a first circuit coupled to the PCI data bus and configured to receive first data, wherein the first circuit is configured to ~~process~~ **format** the first data for subsequent transmission over the PCI data bus;

a second circuit coupled to the first circuit via the PCI data bus, wherein the second circuit is configured to receive second data from the first circuit via the PCI data bus, wherein the second circuit is configured to ~~process~~ **translate** the second data for subsequent transmission over a PCI-Express bus;

wherein the PCI data bus is configured to transmit data between only the first and second circuits.

**Claim 11. (Amended)**

A system comprising:

a first pair of circuits;

a second pair of circuits;

a first PCI data bus, wherein the first PCI data bus **only** transmits data between the first pair of circuits;

a second PCI data bus, wherein the second PCI data bus transmits data between the second pair of circuits;

first and second PCI-Express data buses coupled to one circuit of the first pair and one circuit of the second pair, respectively **to allow communication between the first pair of circuits and the second pair of circuits via the first and second PCI-Express data buses**.

**Claim 15. (Amended)**

An integrated circuit comprising:

a PCI data bus formed on a substrate;

a first sub-circuit formed on the substrate; **wherein the first sub-circuit is configured to receive a first data and translate the first data into PCI formatted data;**

a second sub-circuit formed on the substrate, wherein the sub-second circuit is configured **to receive the PCI formatted data from the first sub-circuit and**

**translate the PCI formatted data into PCI Express formatted data** ~~to transmit data to a PCI-Express bus~~;

wherein the PCI data bus transmits data only between the first and second sub-circuits; wherein the PCI data bus, the first sub-circuit, and the second sub-circuit are integrally formed on the substrate.

**Claim 19. (Amended)**

An apparatus comprising:

a core circuit;

a data bus;

a first circuit coupled to the core circuit via the data bus and configured to receive first data from the core circuit, wherein the first circuit is configured to translate the first data into PCI formatted data;

a PCI data bus;

a second circuit coupled to the first circuit via the PCI data bus, wherein the second circuit is configured to receive the PCI formatted data from the first, wherein the second circuit is configured to translate the PCI formatted data received from the first circuit into PCI-Express formatted data;

**wherein the PCI data bus is configured to transmit data between only the first and second circuits** ~~wherein the core circuit, first circuit, and second circuit comprise the same PCI-Express device~~.